IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application:
Rajeev Joshi et al.

Serial No.: 10/618,113

Filed: July 11, 2003

For: WAFER-LEVEL SHIP SCALE PACKAGE AND METHOD FOR FABRICATING AND USING THE SAME

Confirmation No. 8697

Group Art Unit: 2891

Examiner: David A. Karneke

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

DECLARATION UNDER 37 C.F.R. § 1.132

I, the undersigned, declare the following.

1. I am one of the inventors of the subject matter in the above-captioned patent application.

2. I consider myself "one with ordinary skill in the art" in the semiconductor industry. My qualifications include a Ph. D. degree in aeronautics and astronautics engineering from Purdue University and extensive experience in the semiconductor industry, having worked in electronic packaging for more than 15 years.

3. I have reviewed the claims pending in the U.S. Patent & Trademark Office. I have also reviewed Higgins III (U.S. Patent No. 6,294,405, hereafter "Higgins,") and Chakravorty (U.S. Patent No. 6,350,668) which I have been informed has been cited again the pending claims.

4. I have been informed that the claims have been rejected because the Examiner considers it obvious to omit the UBM (under bump metallization) pad from the Higgins. Column 9, lines 13-16 of Chakravorty describes that the UBM layer is used to ensure good wettability and adhesion of the overlying metal bumps. In light of these functions described in Chakravorty, I would have not considered eliminating the UBM pad from Higgins because these functions would have been lost. As well, I would have not considered eliminating the UBM pad from Higgins because the UBM is required in a solder bump structure to achieve the following functions. First, as a solder diffusion barrier layer, the UBM will provide a diffusion barrier between the solder and bonding pad metallization. Second, as a solder wettable surface, the finial layer of the UBM structure must be solder wettable since this is the layer that bonds to the solder bump. And third, as an oxidation barrier layer, to assure good solderability the UBM must not oxidize solder bump formation process.

5. I have also been informed that some of the claims have been rejected over a combination of Higgins and Chakravorty. The Examiner would combined these two patents by modifying the device of Figure 1 device of Higgins by placing the solder balls (314) of Chakravorty on the stud bumps (20) and then placing the substrate (50) of Higgins on the solder balls (314), thereby locating the solder balls (314) between the stud bumps (20) and the bond pads (52). Such a combination is attached as Exhibit A.

6. The Examiner's combination of adding solder balls between the semiconductor device (11) and substrate (50) of the Higgins reference would result in thicker and less compact semiconductor device than without the combination.

7. Lower inductance would not necessarily result from this combination for two reasons. First, too much solder (in the solder balls 314) would short the adjacent pads and therefore not be

a desired result. Second, the inductance is limited by the cross section of the ball/metal stud/bondpad structure, and having a bunch of overlapping solder certainly wouldn't help the inductance.

8. In this combination, no component of Higgins has been eliminated and, therefore, no process step (for making these components) could have been eliminated. Indeed, the combination would require, at the very least, one additional step of providing the solder balls (314) on the stud bump (20).

9. In the combination, no component of Higgins has been eliminated, so the same number of materials (for making these components) will stills have to be used. Indeed, as shown in Exhibit A, the combination would require more materials (i.e., those needed for the solder balls 314).

10. In the combination, no component of Higgins has been eliminated, so no costs (resulting from these components) have been reduced. Indeed, as shown in Exhibit A, the combination would require more processing steps and more materials (as shown above). Thus, the costs would presumably increase.

11. In the combination shown in Exhibit A, there is no need to add the larger solder ball (314) on the top of small solder ball (20) since the solder ball (314) would rather be used to replace the solder ball (20). As well, adding the solder ball (314) will raise the following issues. First, adding the solder ball (314) will not wet the passivation layer and yet it might also crack the passivation layer due to the high CTE mismatch between the passivation and the solder at high temperature reflow processing. Second, there might not be enough space to add the larger solder ball (314). And third, adding the solder ball (314) will require a reflow which will need another cleaning process to remove the flux residual.

12. That all statements are made of my own knowledge are true and all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

Chung-Lin Wu

9/7/2007

Chung-Lin Wu

Date